

## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for forming an oxide layer having a first thickness in an integrated circuit device process, comprising:  
growing a thermal oxide layer having a second thickness thinner than the first thickness on a surface of a semiconductor substrate in a chemical vapor deposition (CVD) apparatus; and  
forming a CVD oxide layer, after growing the thermal oxide layer, the CVD oxide layer having a third thickness substantially equal to a difference between the first thickness and the second thickness directly on the thermal oxide layer in the same CVD apparatus.
2. (Original) The method of claim 1, wherein the thermal oxide layer is formed to a thickness of approximately 20Å to 100Å.
3. (Previously presented) The method of claim 1, wherein the CVD oxide layer is formed of a material selected from the group consisting of silicon oxide, aluminum oxide, zirconium oxide, and tantalum oxide.
4. (Previously presented) The method of claim 1, further comprising: forming another material layer on the CVD oxide layer in the CVD apparatus.
5. (Previously presented) The method of claim 1, wherein growing a thermal oxide layer comprises using O<sub>2</sub>, N<sub>2</sub>O or a combination thereof for an oxidizing ambient.
6. (Original) The method of claim 1, wherein growing a thermal oxide layer is carried out at a temperature of approximately 750°C to 1000°C.
7. (Previously presented) The method of claim 1, wherein growing a thermal oxide layer is carried out at a temperature of approximately 750°C to 1000°C and forming a CVD oxide layer is carried out at a temperature of approximately 700°C to 850°C.
8. (Previously presented) The method of claim 1, wherein the surface of the semiconductor substrate comprises a bottom and a sidewall of a trench formed by etching the substrate to a predetermined depth; and

wherein the thermal oxide layer is formed to a thickness of approximately 20Å to 100Å, and the CVD oxide layer is formed to a thickness of approximately 50Å to 400Å.

9. (Previously presented) The method of claim 8, wherein the CVD oxide layer is formed of a material selected from the group consisting of silicon oxide, aluminum oxide, zirconium oxide, and tantalum oxide.

10. (Previously presented) The method of claim 8, wherein growing a thermal oxide layer uses O<sub>2</sub>, N<sub>2</sub>O or a combination thereof as a source gas at a temperature of approximately 750°C to 1000°C, and forming a CVD oxide layer is carried out using N<sub>2</sub>O and SiH<sub>4</sub> as source gases at a temperature of approximately 700°C to 850°C.

11. (Previously presented) The method of claim 8, further comprising: forming a nitride liner layer on the CVD oxide layer in the CVD apparatus to a thickness of approximately 30Å to 100Å, and forming a trench filling layer on the nitride liner layer in the CVD apparatus to a thickness of approximately 3000Å to 10000Å.

12. (Currently Amended) A method of forming an oxide layer having a first thickness in an integrated circuit device process, comprising:

forming a thermal oxide layer having a second thickness thinner than the first thickness on an exposed single crystalline silicon substrate in a chemical vapor deposition (CVD) apparatus; and

forming a CVD oxide layer, after forming the thermal oxide layer, the CVD oxide layer having a third thickness substantially equal to the differential thickness between the first thickness and the second thickness directly on the thermal oxide layer in the same CVD apparatus,

wherein a thickness of approximately 8.8 Å to 44 Å of the exposed single crystalline silicon substrate is consumed during the forming of the thermal oxide layer.

13. (Previously presented) The method of claim 12, wherein forming a thermal oxide layer is carried out at a temperature of approximately 750°C to 1000°C, and forming a CVD oxide layer is carried out at a temperature of approximately 700°C to 850°C.

14. (Previously presented) The method of claim 13, wherein O<sub>2</sub>, N<sub>2</sub>O or combination thereof is used as a source gas for forming a thermal oxide layer, and N<sub>2</sub>O and SiH<sub>4</sub> are used as a source gas for forming a CVD oxide layer.

15. (Previously presented) A method of forming a layer for an integrated circuit device, comprising:

forming a trench in a single crystalline silicon substrate by etching;

forming an oxide layer of a double layer structure with a first thickness on a surface of the trench;

forming a nitride liner layer on the oxide layer,

wherein forming the oxide layer comprises:

forming a thermal oxide layer having a second thickness of 20 Å to 100 Å on the trench;

forming a CVD conformal liner material layer having a third thickness substantially equal to a difference between the first thickness and the second thickness directly on the oxide layer,

wherein the thermal oxide layer, the liner material layer, and the nitride liner layer are formed in the same chemical vapor deposition (CVD) apparatus,

and wherein a thickness of 8.8 Å to 44 Å of single crystalline silicon substrate is consumed during the forming of the thermal oxide layer.

16. (Cancelled)

17. (Original) The method of claim 15, wherein the liner material layer is formed to a thickness of 50Å to 400Å.

18. (Original) The method of claim 15, wherein the liner material layer is made of a material selected from the group consisting of silicon dioxide, aluminum trioxide, zirconium oxide, and tantalum pentoxide.

19. (Cancelled)

20. (Previously presented) The method of claim 15, wherein the thermal oxide layer is formed using O<sub>2</sub>, N<sub>2</sub>O or a combination thereof as a source gas at a temperature of approximately 750°C to 1000°C, and the liner material layer is a high temperature oxide layer

formed using  $\text{N}_2\text{O}$  and  $\text{SiH}_4$  as a source gas at a temperature of approximately  $700^\circ\text{C}$  to  $850^\circ\text{C}$ .

21. (Original) The method of claim 20, further comprising: forming a trench isolation material on the nitride liner layer in the same CVD apparatus to fill the trench.

22. (Previously presented) A method of forming an isolation trench, comprising, etching a single crystalline silicon substrate to form a trench therein; forming an oxide layer having a double layer structure with a first thickness on a surface of the trench;

forming a nitride liner layer on the oxide layer; and,

forming a trench isolation material layer on the nitride liner layer to fill the trench, wherein forming the oxide layer comprises:

forming a thermal oxide layer having a second thickness of  $20 \text{ \AA}$  to  $100 \text{ \AA}$  on the trench;

forming a CVD conformal liner material layer having a third thickness substantially equal to a difference between the first thickness and the second thickness directly on the oxide layer,

wherein the thermal oxide layer, the conformal liner material layer, and the nitride liner layer, and the trench isolation layer are formed in the same chemical vapor deposition (CVD) apparatus,

and wherein a thickness of  $8.8 \text{ \AA}$  to  $44 \text{ \AA}$  of single crystalline silicon substrate is consumed during the forming of the thermal oxide layer.

23. (Cancelled)

24. (Previously presented) The method of claim 22, wherein the material barrier layer is formed to a thickness of  $50 \text{ \AA}$  to  $400 \text{ \AA}$ .

25. (Previously presented) The method of claim 22, wherein the thermal oxide layer is formed using  $\text{O}_2$ ,  $\text{N}_2\text{O}$  a combination thereof as a source gas at a temperature of approximately  $750^\circ\text{C}$  to  $1000^\circ\text{C}$ , and the liner material layer is a higher temperature oxide layer formed using  $\text{N}_2\text{O}$  and  $\text{SiH}_4$  as a source gas at a temperature of approximately  $700^\circ\text{C}$  to  $850^\circ\text{C}$ .

26. (Previously presented) The method of claim 22, wherein the liner material layer is made of a material selected from the group consisting of silicon oxide, aluminum oxide, zirconium oxide, and tantalum oxide.

27. (Withdrawn) A trench isolation structure comprising:  
a trench for device isolation formed in a semiconductor substrate to a predetermined depth;  
a thermal oxide layer formed on a bottom and a sidewall of the trench to a thickness of 20Å to 100Å;  
a chemical vapor deposition (CVD) material barrier layer formed on the thermal oxide layer to a thickness of 50Å to 400Å;  
a nitride liner layer formed on the CVD material barrier layer; and  
a trench isolation material layer formed on the nitride liner layer to fill up the trench.

28. (Withdrawn) The trench isolation structure of claim 27, wherein thermal oxide layer and the CVD material barrier layer are formed in the same CVD apparatus, and the CVD material barrier layer is made of aluminum oxide.